



MOTOROLA

SEMICONDUCTORS

3501 ED BLUESTEIN BLVD. AUSTIN, TEXAS 78721

021004

MCM4517

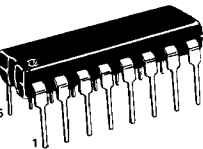
16,384-BIT DYNAMIC RAM

The MCM4517 is a 16,384-bit, high-speed, dynamic Random-Access Memory. Organized as 16,384 one-bit words and fabricated using HMOS high performance, N channel, silicon-gate technology. This new breed of 5-volt only dynamic RAM combines high performance with low cost and improved reliability.

By multiplexing row and column-address inputs, the MCM4517 requires only seven address lines and permits packaging in standard 16-pin dual-in-line packages. Complete address decoding is done on chip with address latches incorporated. Data out is controlled by $\overline{\text{CAS}}$ allowing for greater system flexibility.

All inputs and outputs, including clocks, are fully TTL compatible. The MCM4517 incorporates a one-transistor cell design and dynamic storage techniques.

- Organized as 16,384 Words of 1 Bit
- Single +5 Volt Operation
- Fast 100 ns Operation
- Low Power Dissipation:
 - 170 mW Maximum (Active) *S-2*
 - 14 mW Maximum (Standby)
- Maximum Access Time *003290*
 - MCM4517 10' 100 ns
 - MCM4517 12' 120 ns *T-3290*
 - MCM4517 15' 150 ns
 - MCM4517 20' 200 ns
- Three-State Data Output
- Internal Latches for Address and Data Input
- Early-Write Common I/O Output Capability
- 64K Compatible 128-cycle, 2 ms Refresh
- $\overline{\text{RAS}}$ -only Refresh Mode
- $\overline{\text{CAS}}$ Controlled Output
- Upward Pin Compatibility from the 16K RAM (MCM4116) to the 64K RAM (MCM6664)
- Allows Undershoot $V_{IL \text{ min}} = -2 \text{ V}$
- Hidden $\overline{\text{RAS}}$ Only Refresh Capability

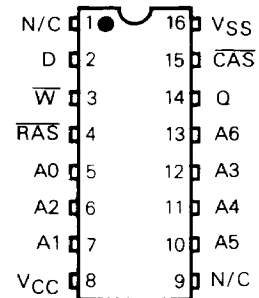


OR16

P SUFFIX
PLASTIC PACKAGE
CASE 648

MOT

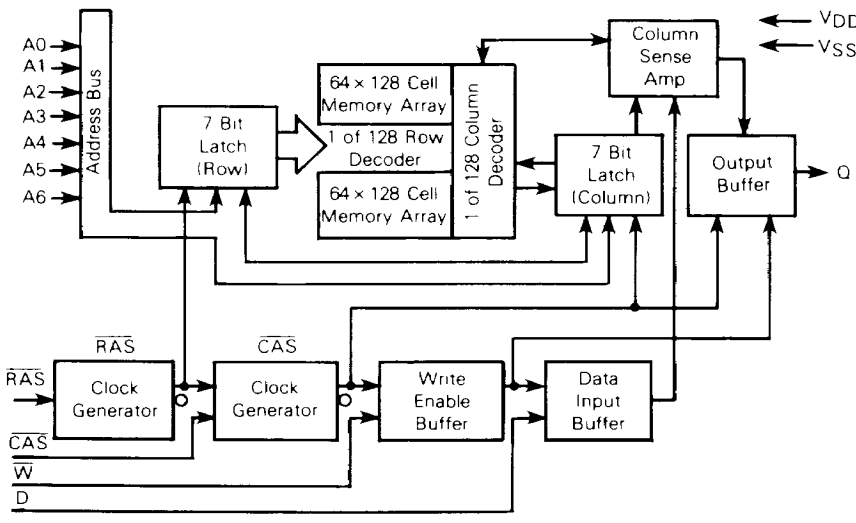
PIN ASSIGNMENT



PIN NAMES

A ₀ -A ₆	Address Input
D	Data In
Q	Data Out
$\overline{\text{W}}$	Read/Write Input
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
V _{CC}	Power (+5 V)
V _{SS}	Ground

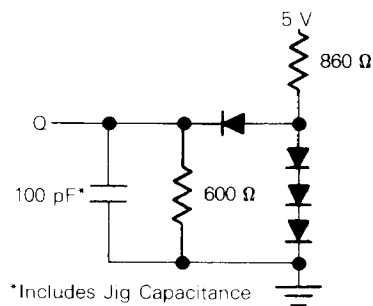
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to V _{SS}	V _{in} , V _{out}	-2 to +7	V _{dc}
Operating Temperature Range	T _A	0 to +70	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C
Power Dissipation	P _D	1.0	W
Data Out Current	I _{out}	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

FIGURE 1 — OUTPUT LOAD


*Includes Jig Capacitance

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full Operating Voltage and Temperature Range Unless Otherwise Noted.)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	V _{CC} V _{SS}	4.5 0	5.0 0	5.5 0	V	1
Logic 1 Voltage, All Inputs	V _{IH}	2.4	—	V _{CC} +1	V	1
Logic 0 Voltage, All Inputs	V _{IL}	-2.0	—	0.8	V	1

DC CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Units	Notes
V _{CC} Supply Current (Standby)	I _{CC1}	—	1.8	2.5	mA	5
V _{CC} Supply Current (Operating) 4517-10, t _{RC} = 235 4517-12, t _{RC} = 270 4517-15, t _{RC} = 320 4517-20, t _{RC} = 350	I _{CC2}	—	22 20 18 16	31 28 25 23	mA	4
V _{CC} Supply Current (RAS-Only Cycle) 4517-10, t _{RC} = 235 4517-12, t _{RC} = 270 4517-15, t _{RC} = 320 4517-20, t _{RC} = 350	I _{CC3}	—	14 12 11 10	23 21 19 18	mA	4
V _{CC} Standby Current (Standby, Output Enable) (CAS at V _{IL} , RAS at V _{IH})	I _{CC4}	—	2	5	mA	
V _{CC} Supply Current (Page Mode Cycle Only) 4517-10, t _{RC} = 235 4517-12, t _{RC} = 270 4517-15, t _{RC} = 320 4517-20, t _{RC} = 350	I _{CC5}	—	17 15 13 10	23 21 18 15	mA	
Input Leakage Current (Any Input) (V _{SS} ≤ V _{in} ≤ V _{CC})	I _{I(L)}	—	—	10	μA	
Output Leakage Current (0 ≤ V _{out} ≤ 5.5) (CAS at Logic 1)	I _{O(L)}	—	—	10	μA	
Output Logic 1 Voltage@I _{out} = -4 mA	V _{OH}	2.4	—	—	V	
Output Logic 0 Voltage@I _{out} = 4 mA	V _{OL}	—	—	0.4	V	

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full Operating Voltage and Temperature Range Unless Otherwise Noted)

(See Notes 2, 3, 9, 14 and Figure 1)

Parameter	Symbol	MCM4517-10		MCM4517-12		MCM4517-15		MCM4517-20		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t _{RC}	235	—	270	—	320	—	360	—	ns	8, 9
Read-Modify-Write Cycle Time	t _{RWC}	285	—	320	—	410	—	440	—	ns	8, 9
Access Time from Row Address Strobe	t _{RAC}	—	100	—	120	—	150	—	200	ns	10, 12
Access Time from Column Address Strobe	t _{CAC}	—	55	—	65	—	80	—	120	ns	11, 12
Output Buffer and Turn-Off Delay	t _{OFF}	0	45	0	50	0	60	0	70	ns	18
Row Address Strobe Precharge Time	t _{RP}	110	—	120	—	135	—	150	—	ns	
Row Address Strobe Pulse Width	t _{RAS}	115	10000	140	10000	175	10000	200	10000	ns	19
Column Address Strobe Pulse Width	t _{CAS}	55	10000	65	10000	95	10000	120	10000	ns	19
Row to Column Strobe Lead Time	t _{RCD}	25	45	25	55	25	70	30	80	ns	13
Row Address Setup Time	t _{ASR}	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t _{RAH}	15	—	15	—	20	—	25	—	ns	
Column Address Setup Time	t _{ASC}	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t _{CAH}	15	—	15	—	20	—	20	—	ns	
Column Address Hold Time Referenced to RAS	t _{AR}	60	—	70	—	90	—	140	—	ns	
Transition Time (Rise and Fall)	t _T	3	50	3	50	3	50	3	50	ns	6



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AC OPERATING CONDITIONS AND CHARACTERISTICS (Continued)

Parameter	Symbol	MCM4517-10		MCM4517-12		MCM4517-15		MCM4517-20		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Command Setup Time	t _{RCS}	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time	t _{RCH}	0	—	0	—	0	—	0	—	ns	14
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t _{RRH}	20	—	25	—	35	—	40	—	ns	14
Write Command Hold Time	t _{WCH}	25	—	30	—	45	—	60	—	ns	
Write Command Hold Time Referenced to $\overline{\text{RAS}}$	t _{WCR}	70	—	85	—	115	—	140	—	ns	
Write Command Pulse Width	t _{WP}	25	—	30	—	50	—	50	—	ns	
Write Command to Row Strobe Lead Time	t _{RWL}	60	—	65	—	110	—	110	—	ns	
Write Command to Column Strobe Lead Time	t _{CWL}	45	—	50	—	100	—	100	—	ns	
Data in Setup Time	t _{DS}	0	—	0	—	0	—	0	—	ns	15
Data in Hold Time	t _{DH}	25	—	30	—	45	—	60	—	ns	15
Data in Hold Time Referenced to $\overline{\text{RAS}}$	t _{DHR}	70	—	85	—	115	—	140	—	ns	
Column to Row Strobe Precharge Time	t _{CRP}	0	—	0	—	0	—	0	—	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	70	—	85	—	105	—	120	—	ns	
Refresh Period	t _{REFSH}	—	2.0	—	2.0	—	2.0	—	2.0	ms	
Write Command Setup Time	t _{WCS}	0	—	0	—	0	—	0	—	ns	16
$\overline{\text{CAS}}$ to $\overline{\text{WRITE}}$ Delay	t _{CWD}	55	—	65	—	80	—	100	—	ns	16
$\overline{\text{RAS}}$ to $\overline{\text{WRITE}}$ Delay	t _{RWD}	100	—	120	—	150	—	160	—	ns	16
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	100	—	120	—	165	—	200	—	ns	
$\overline{\text{CAS}}$ Precharge, Non Page Mode	t _{CPN}	50	—	55	—	70	—	90	—	ns	
RMW Cycle $\overline{\text{RAS}}$ Pulse Width	t _{RRW}	135	10000	160	10000	195	10000	220	10000	ns	
RMW Cycle $\overline{\text{CAS}}$ Pulse Width	t _{CRW}	95	10000	110	10000	130	10000	140	10000	ns	
Page Mode Cycle Time	t _{PC}	125	—	145	—	190	—	260	—	ns	
Page Mode Cycle Time (Read-Modify-Write)	t _{PCM}	175	—	200	—	280	—	360	—	ns	
$\overline{\text{CAS}}$ Precharge Time (Page Mode Cycle Only)	t _{CP}	60	—	70	—	85	—	105	—	ns	
$\overline{\text{RAS}}$ Pulse Width (Page Mode Cycle Only)	t _{RPM}	115	10000	140	10000	175	10000	235	10000	ns	

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = +5 V. Periodically sampled rather than 100% tested.)

Parameter	Symbol	Typ	Max	Units	Notes
Input Capacitance (A0-A6), D _{in}	C _{I1}	4.0	5.0	pF	7
Input Capacitance $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WRITE}}$	C _{I2}	5.0	7.0	pF	7

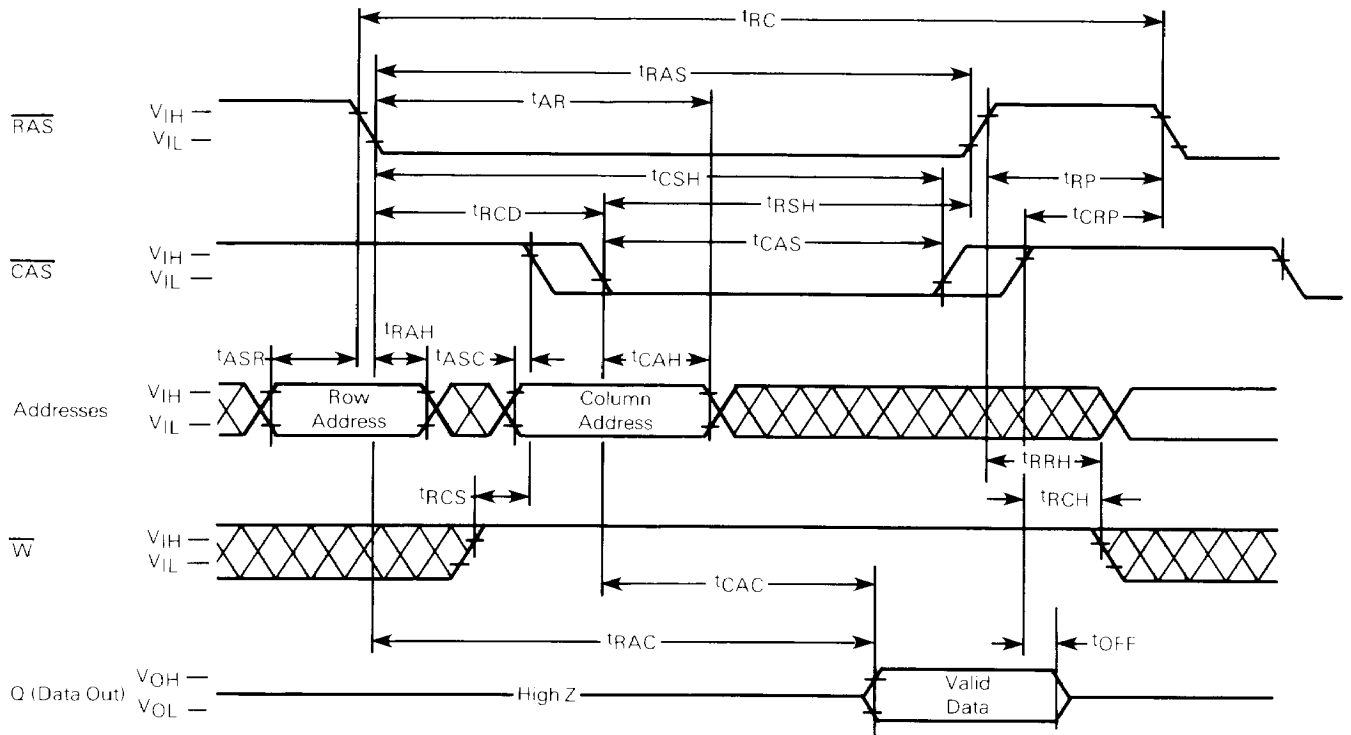
NOTES:

- All voltages referenced to V_{SS}.
- V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
- An initial pause of 100 μs is required after power-up followed by any 8 $\overline{\text{RAS}}$ cycles before proper device operation guaranteed.
- Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
- Output is disabled (open-circuit) and $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are both at a logic 1.
- The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transmit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
- Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I_Δ/ΔV
- The specifications for t_{RC} (min), and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
- AC measurements assume t_T = 5.0 ns.
- Assumes that t_{RCD} ≤ t_{RCD} (Max)
- Assumes that t_{RCD} ≥ t_{RCD} (Max)
- Measured with a current load equivalent to 2 TTL loads (+ 200 μA, - 4 mA) and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).
- Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
- Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
- These parameters are referenced to $\overline{\text{CAS}}$ leading edge in random write cycles and to $\overline{\text{WRITE}}$ leading edge in delayed write or read-modify-write cycles.
- t_{WCS}, t_{CWD}, and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if t_{WCS} ≥ t_{WCS} (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if t_{CWD} ≥ t_{CWD} (min) and t_{RWD} ≥ t_{RWD} (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
- Addresses, data-in and $\overline{\text{WRITE}}$ are don't care. Data-out depends on the state of $\overline{\text{CAS}}$. If $\overline{\text{CAS}}$ remains low, the previous output will remain valid. $\overline{\text{CAS}}$ is allowed to make an active to inactive transition during the $\overline{\text{RAS}}$ -only refresh cycle. When $\overline{\text{CAS}}$ is brought high, the output will assume a high-impedance state.
- t_{off} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- For read and write cycles only.

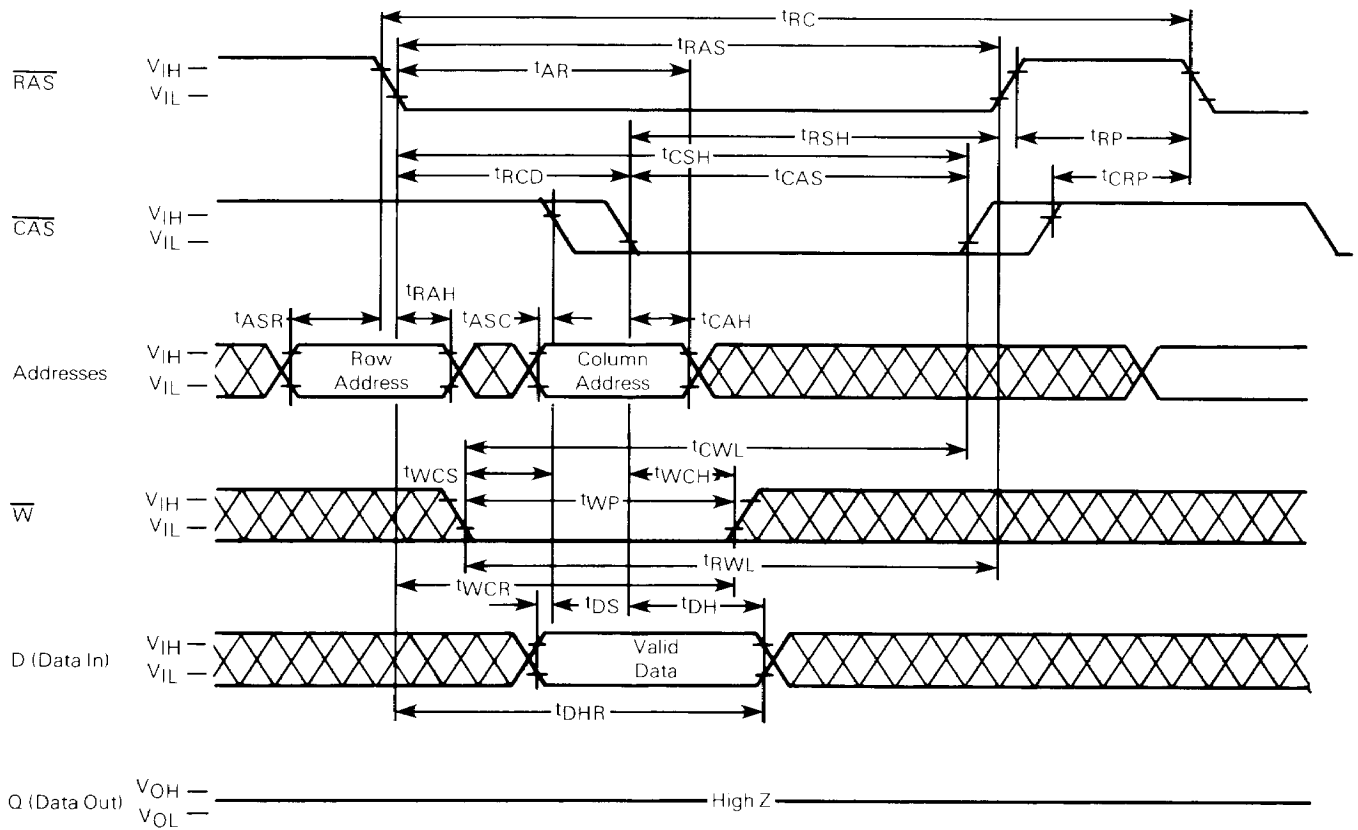


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READ CYCLE TIMING

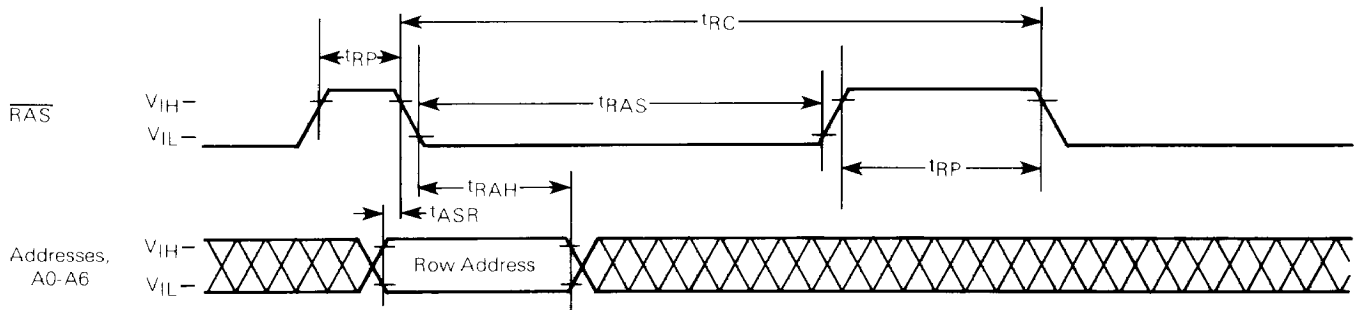


WRITE CYCLE TIMING

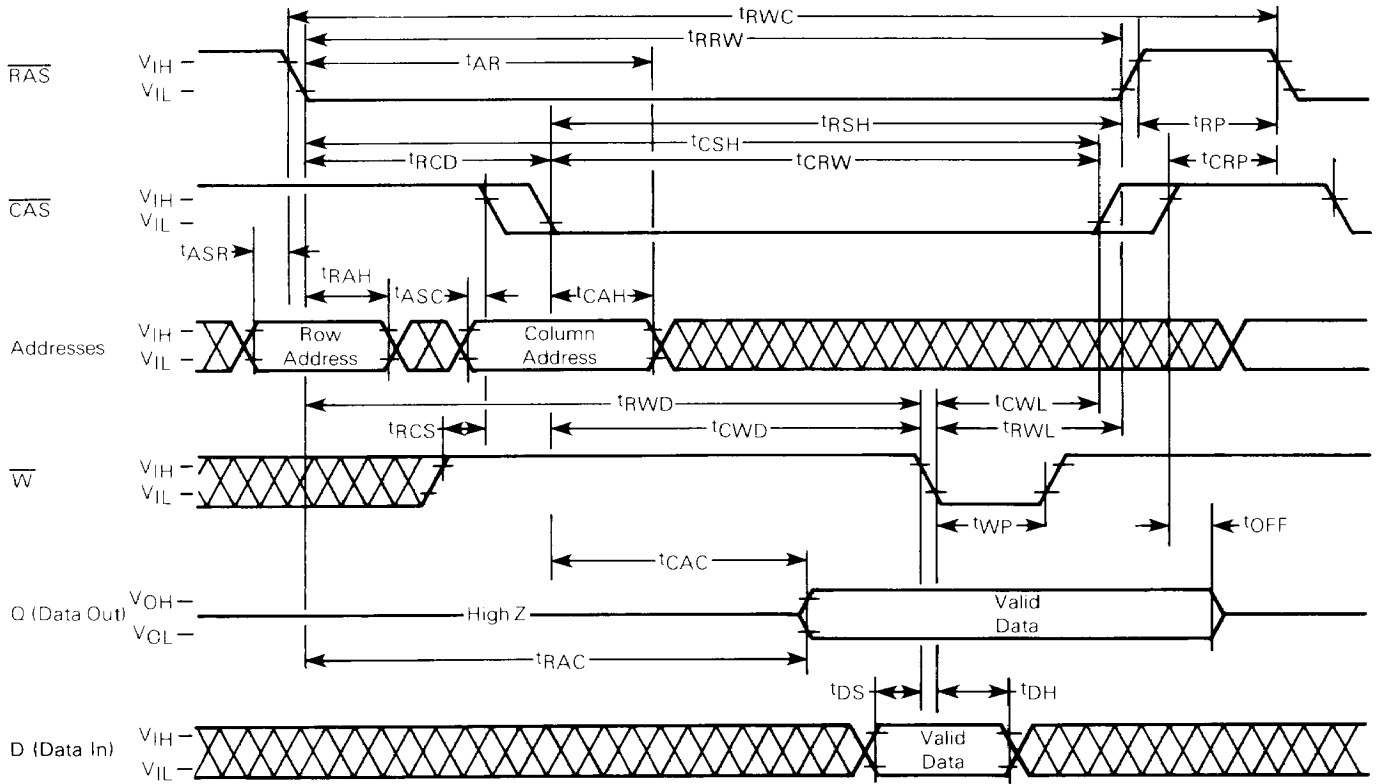


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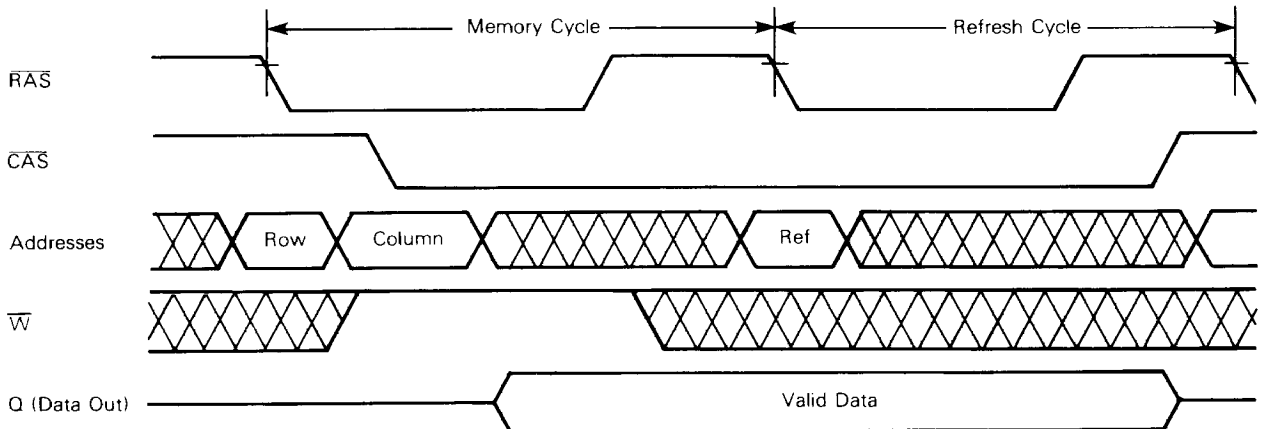
RAS-ONLY REFRESH CYCLE
 (Data-In and Write are Don't Care, CAS is HIGH)



READ-WRITE/READ-MODIFY-WRITE CYCLE

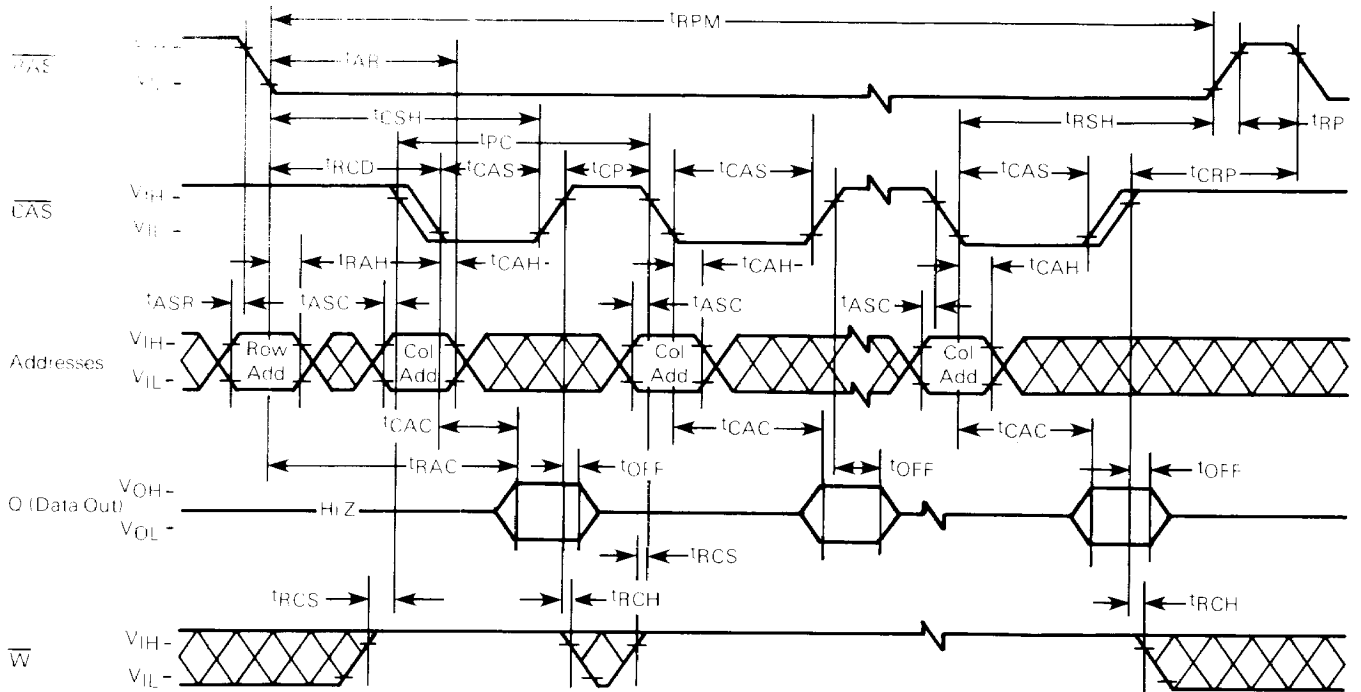


HIDDEN RAS-ONLY REFRESH CYCLE

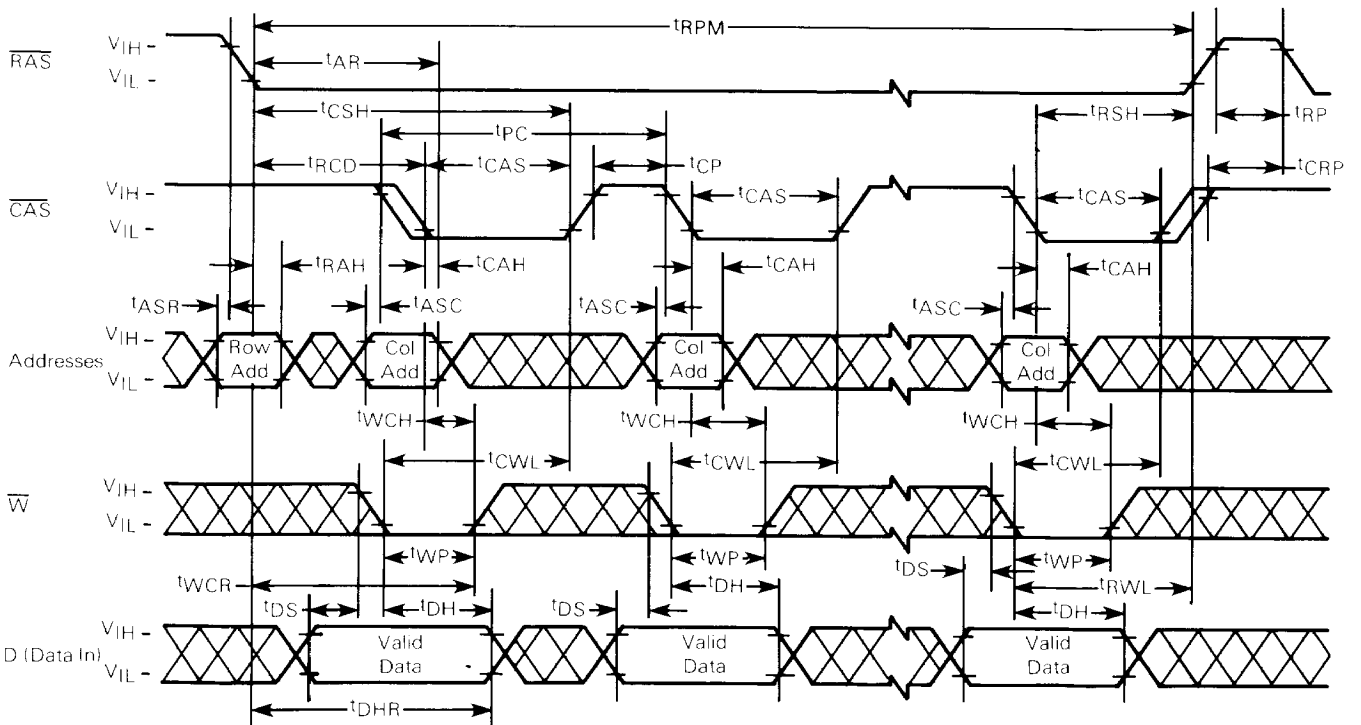


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PAGE MODE READ CYCLE

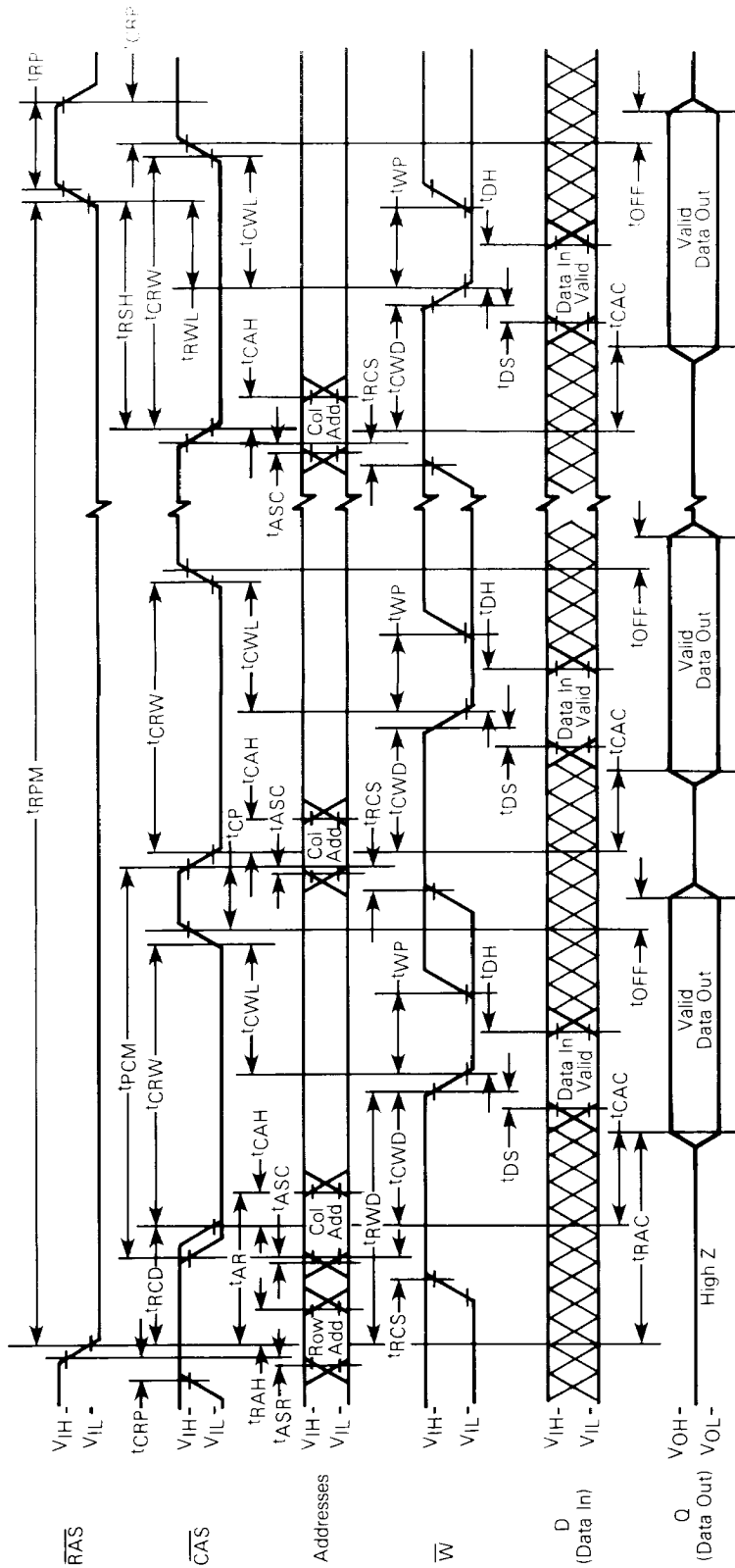


PAGE MODE WRITE CYCLE



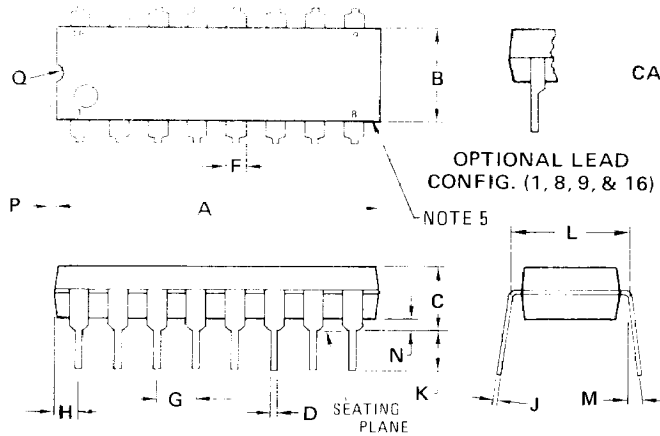
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PAGE MODE READ-MODIFY-WRITE CYCLE



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PACKAGE DIMENSIONS



CASE 648-05

OPTIONAL LEAD CONFIG. (1, 8, 9, & 16)

NOTE 5

NOTES:

1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 8, 9, and 16).
5. ROUNDED CORNERS OPTIONAL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	21.34	0.740	0.840
B	6.10	6.60	0.240	0.260
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.38	2.41	0.015	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

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